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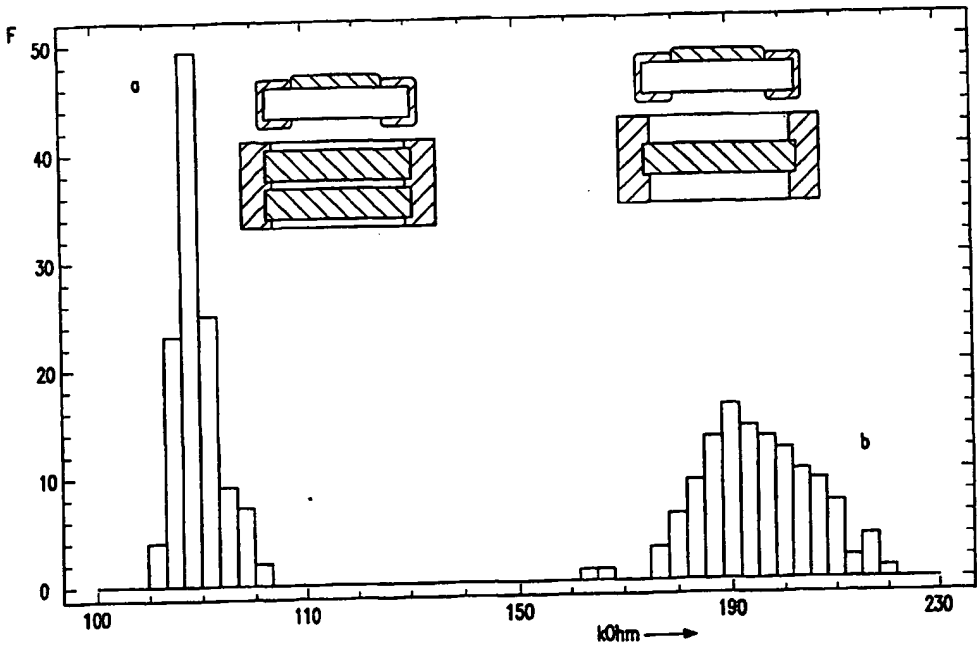
(54) Title: THICK FILM CHIP RESISTOR AND ITS MANUFACTURE



(57) Abstract

An improved method of manufacturing thick film chip resistors in mass production is described. By applying two or more resistance layers per chip resistor, less variance in the eventual resistance value is obtained if the resistors are manufactured in mass production using substrate plates. Less variance in the resistance value implies less trimming activity, which leads to a considerable cost reduction. Moreover, the use of two or more sub–layers enables application of TCR compensation by applying a resistive material having a positive

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Thick film chip resistor and its manufacture.

The invention relates to a method of manufacturing thick film chip resistors, said method comprising the following steps:

a. providing a number of contact layers on an electrically insulating substrate plate,

b. applying a number of thick film resistance layers on the substrate plate, each of said thick film resistance layers being in contact with two neighbouring contact layers,

c. fracturing the substrate plate into substrate rods,

d. applying end contacts to the contact layers, and

e. fracturing the rods into individual thick film resistors.

The invention also relates to a thick film chip resistor comprising an electrically insulating substrate a main surface of which is provided with two contact layers between which a thick film resistance layer is provided, each of said contact layers being provided with an end contact.

Both a method of manufacturing thick film chip resistors of the type mentioned in the opening paragraph and thick film chip resistors thus manufactured are known as such, f.i. from the American Patent Specification US 5.258.738 in the name of Applicant. This prior art document describes the use of alumina substrates of a specific type, which provides the fractured substrate rods so-called 'intergranular' fracture surfaces. The presence of such surfaces results in a better bonding between the substrate and the end contacts.

The known method of manufacturing thick film chip resistors suffers from an important disadvantage. It appears that the resistance values of the individual chip resistors which are obtained from a substrate plate are not (almost) identical, but show a certain variance around a mean resistance value. In order to obtain resistors with (almost) identical resistance values, a so-called trimming step is necessary. By trimming a small amount of the resistance material is removed, preferably by means of a laser, from the

resistance layer. Measuring the resistance value of the individual resistors and trimming them to a desired (higher) value results in resistors having (almost) identical resistance values. However, such trimming step is rather time-consuming and costly, and the trimming activity should therefor be as small as possible.

The main purpose of the invention is to reduce the mentioned disadvantage. The invention specifically aims at providing a method as mentioned in the opening paragraph, wherein the resistance values of individual thick film chip resistors obtained from one substrate plate show less variance around a desired resistance value.

These and other objects of the present invention are achieved by means of the method mentioned in the opening paragraph, which method in accordance with the invention is characterized in that the thick film resistance layer of each individual thick film chip resistor comprises at least two separate sub layers.

Experimental results have shown that separating the single thick film resistance layer as described in the prior art document into two or more sub layers results in a lower variance of the resistance values of the resistors around a certain mean value. This favourable effect causes a considerable reduction of the required trimming time and therefore results in a significant cost reduction of the known mass production process.

A favourable embodiment of the inventive method is characterized in that contact layers and thick film resistance layers are provided on both main surfaces of the substrate plate. This measure causes an advantageous increase of the power dissipation of thick film chip resistors having the same dimensions and electrical specifications. Chip resistors of the preferred construction can therefor better withstand high power applications.

Another favourable embodiment of the inventive method is characterized in that at least one of the sub layers comprises a resistive material having a positive TCR and in that at least one of the sub layers comprises a resistive material having a negative TCR. Thick film chip resistors of today generally suffer from the disadvantage that the absolute value of the TCR (temperature coefficient of the resistance) is rather high, typically 100 ppm/°C or more. For so-called low-ohmic resistors having a resistance value of 50 mΩ or less which are manufactured by thick film technology, the high TCR value of 500 ppm/°C or more causes an even more serious problem. By applying the proposed measure, TCR compensation is possible by using for a first sub layer a resistive material having a positive TCR and for a second sub layer a resistive material having a negative TCR. The TCR value

of the chip resistor will be between the TCR value of the individual sub layers.

The invention also relates to a thick film chip resistor comprising an insulating substrate a main surface of which is provided with two contact layers between which a thick film resistance layer is provided, each of said contact layers being contacted with an end contact. The inventive resistor is characterized in that the thick film resistance layer comprises at least two separate sub layers, which are at a distance of at least 0.05 mm. Using a smaller distance can result in undesired electrical contacts between the sub layers.

Preferably both main surfaces of the substrate are provided with a thick film resistance layer consisting of at least two separate sub layers, which are at a distance of at least 0.05 mm. Another favourable embodiment of the inventive resistor is characterized in that at least one of the sub layers comprises a resistive material having a positive TCR and in that at least one of the sub layers comprises a resistive material having a negative TCR.

The invention will be described in more detail by means of embodiments and the accompanying drawing, wherein

Figures 1 schematically shows different stages in the method according to the present invention

Figure 2 shows in a perspective view a detail of the substrate plate depicted in Figure 1

Figure 3 schematically shows a number of thick film chip resistors according to the present invention

Figure 4 shows in a histogram the results of the variance in resistance value which is measured in mass produced thick film chip resistors which are either manufactured in accordance with the present invention (a) or manufactured not in accordance with the present invention (b).

It is noted that the Figures are not drawn to scale.

The inventive method is described in more detail by means of Figs 1 and 2. Fig 1-A shows a top view of a substrate plate (1) of sintered Al_2O_3 having dimensions of about 108 x 78 x 0.54 mm^3. As shown in Fig 2, the substrate plate has been provided on the bottom surface with a first number of parallel, V-shaped fracture grooves (2) (rod grooves) and with a second number of parallel, V-shaped fracture grooves (3) (chip grooves). The

fracture grooves (2) and (3) extend substantially perpendicularly to each other and have a depth of approximately 0.1 mm. For clarity, only a few fracture grooves (2) and (3) are indicated with a dotted line in Fig 1.

On one of the main surfaces of substrate plate (1) as shown in Fig 1-A, longitudinal contact layers (4) (see Fig 2) are provided. These layers (4) can be provided by means of vacuum deposition techniques, such as f.i. sputtering and metal evaporation, but they are preferably provided by means of screen printing. Said screen printed contact layers, which contain for example Ag or Pd/Ag, are fired at 850° C for 1 hour. For clarity, only three contact layers are shown in Fig 2. It is noted, that the contact layers can also be constructed as small, discrete area's as shown in US 5.258.738.

Subsequently, thick film resistance layers are provided by means of screen printing, which layers are also fired at 850° C for 1 hour. The screen printing paste used for this purpose contains a mixture of conductive material (metal oxides as f.i. RuO_2 and/or $Pb_2Ru_2O_{6.5}$), glass fritt and minor additives such as binders. The resistance value of the resistance layer strongly depend of the exact composition of said paste.

According to an essential aspect of the present invention, these resistance layers comprise at least two separate sub layers (5,8) per individual chip resistor unit. For clarity, only two thick film resistance layers, each comprising two sub layers (5) and (8) per individual chip resistor unit are shown in Fig 2. It is noted that in principle the row order of steps a (providing contact layers) and step b (applying thick film resistance layers) can be reversed. However, the method in which the contact layers are provided on the substrate before the thick film resistance layer are applied is preferred.

In case that both sub layers contain the same resistance material, these layers can be printed in one and the same screen print step. However, according to a preferred embodiment of the present invention, the two sub layers are provided in two different print screen steps, using two types of resistance material. In the preferred embodiment, the one material comprises a resistive material having a positive TCR and the other material comprises a resistive material having a negative TCR. By using this embodiment of the invention, the TCR of the thick film chip resistor is relatively low, which is seen as an important advantage.

According to another preferred embodiment of the present invention, the same procedure of applying contact layers and resistance layers comprising at least two sub layers is also executed on the other main surface of the substrate plate.

After the contact layers and the thick film resistance layers have been

provided on one or both of the main surfaces of the substrate plate (1), a protective coating covering the resistance layers can be applied, f.i. by screen printing (not shown). Subsequently the substrate plate (1) is broken at the fracture grooves (2) (rod grooves) to form rods (6) (see Fig. 1-B). Next, a thin layer of Ni is deposited on the fracture surfaces by means of a vacuum deposition technique, such as f.i. evaporation or sputtering. Subsequently, a thicker layer of Ni is provided on said first layer by means of electroplating and a solder layer is applied onto the Ni-layers. It is also possible to use a dipping process for this purpose by dipping the fracture surfaces into a conductive paste which contains f.i. Ag or Ag/Pd, so that the fracture surfaces become covered by such paste. In such dipping process the substrate rods need to be fired for one hour at about 580°C in order to consolidate the conductive paste as a layer on the fracture surfaces. The thus formed end contacts are electrically conductively connected to the contact layers (4). Finally, the rods (6) are broken along the fracture grooves (3) (chip grooves) into individual thick film chip resistors. In Fig. 1-C, only a few of these resistors are schematically shown. In total, approximately 1800 thick film chip resistors having dimensions of 1.6 x 3.2 x 0.54 mm^3 can be manufactured from said Al_2O_3 substrate.

Fig 3 shows a cross sectional view and a top view of several types of thick film chip resistors, most of them according to the present invention. These resistors comprise an electrically insulating substrate (11) of alumina. Contact layers (12) and thick film resistance layers comprising at least two separate sub layers (vide infra) are present on one or both main surfaces of substrate (11) as depicted in Fig 3-A resp. Fig 4-B. A screen printed protective layer (13) fully cover the resistance layer. U-shaped metallic end contacts (14) are in electrical contact with contact layers (12).

Figs 3-C, 3-D, 3-E and 3-F give a top view of the resistor type as shown in Figs 3-A and 3-B. For clarity, the protective layer (13) is omitted in Figs 3-C, 3-D, 3-E and 3-F. As shown in these Figs, the resistance layer of various embodiments according to the present invention comprise respectively two, three or even four sub layers (15,16,17,18) having a thickness of about 10 micrometer. These layers are at a distance of at least 0.05 mm in order to avoid undesired electrical contact between neighbouring sub layers. The embodiment according to Fig 3-C having only a single resistance layer is not according to the present invention.

Figure 4 shows a histogram in which the frequency (F) of the individual resistors having a certain resistance value (kΩ) is depicted. For this experiment 120 resistors of the type shown in Fig 3-A were manufactured, either according to the presently claimed

inventive method (series a, left histogram) or not according to the present invention (series b, right histogram). The standard deviation of the a-series was about 4.4%. The standard deviation of the b-series was about 5.2%. These results (an 20% improvement) unambiguously demonstrate the effect of the present invention.

In summary, the present invention provides an improved method of manufacturing thick film chip resistors in mass production. By applying two or more resistance layers per chip resistor, less variance in the eventual resistance value is obtained if the resistors are manufactured in mass production using substrate plates. Less variance in the resistance value implies less trimming activity, which leads to a considerable cost reduction. Moreover, the use of two or more sub layers enables application of TCR compensation.

CLAIMS:

1. Method of manufacturing thick film chip resistors, said method comprising the following steps:

a. providing a number of contact layers on an electrically insulating substrate plate,

b. applying a number of thick film resistance layers on the substrate plate, each of said thick film resistance layers being in contact with two neighbouring contact layers,

c. fracturing the substrate plate into substrate rods,

d. applying end contact to the contact layers, and

e. fracturing the rods into individual thick film chip resistors,

characterized in that the thick film resistance layer of each individual thick film chip resistor comprises at least two separate sub layers.

2. Method according to claim 1, characterized in that contact layers and thick film resistance layers are provided on both main surfaces of the substrate plate.

3. Method according to claim 1 or 2, characterized in that at least one of the sub layers of the thick film resistance layer comprises a resistive material having a positive TCR and in that at least one of the sub layers comprises a resistive material having a negative TCR.

4. Thick film chip resistor comprising an electrically insulating substrate a main surface of which is provided with two contact layers between which a thick film resistance layer is provided, each of said contact layers being provided with an end contact, characterized in that the thick film resistance layer comprises at least two separate sub layers, which are at a distance of at least 0.05 mm.

5. Thick film chip resistor as defined in claim 4, characterized in that both main surfaces of the substrate are provided with a thick film resistance layer comprising at least two separate sub layers, which are at a distance of at least 0.05 mm.

6. Thick film chip resistor as defined in claim 4 or 5, characterized in that at least one of the sub layers comprises a resistive material having a positive TCR and in that at least one of the sub layers comprises a resistive material having a negative TCR.

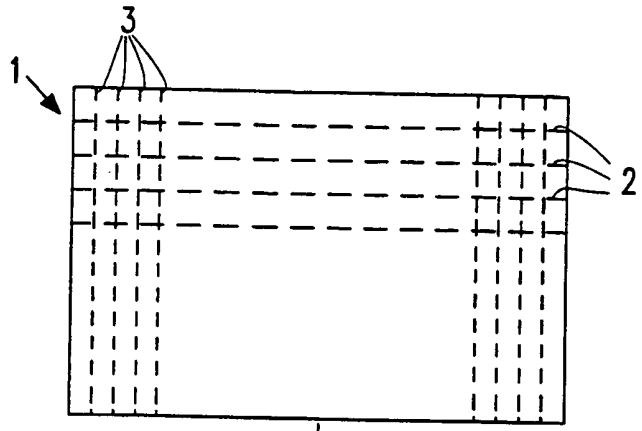

FIG. 1A

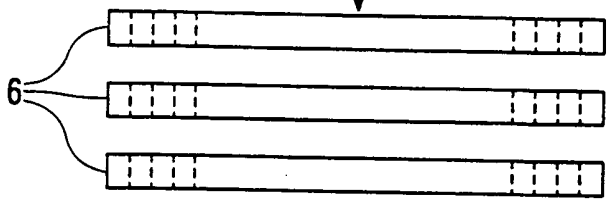

FIG. 1B

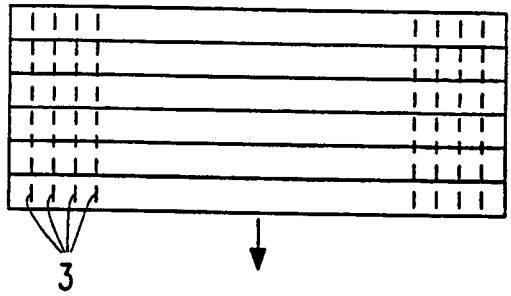

FIG. 1C

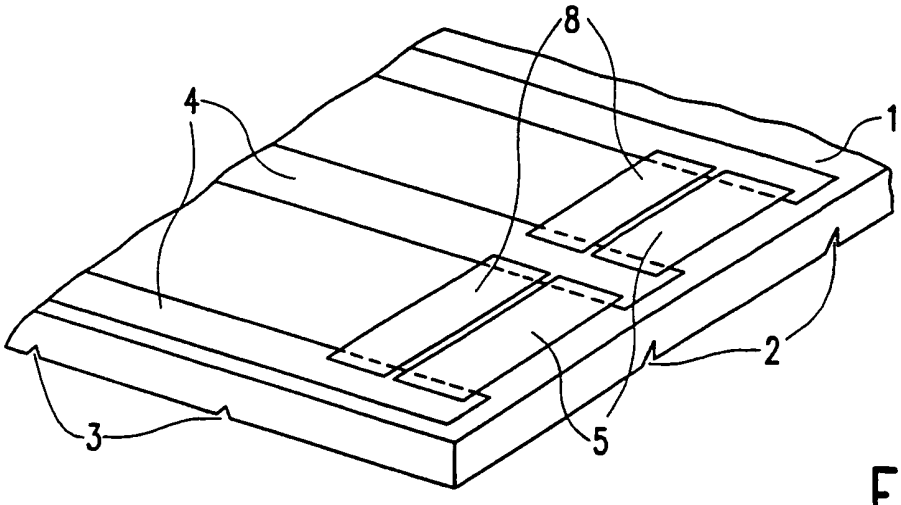

FIG. 2

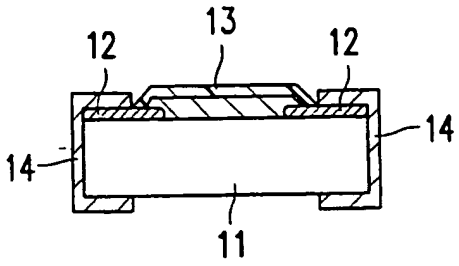

FIG. 3A

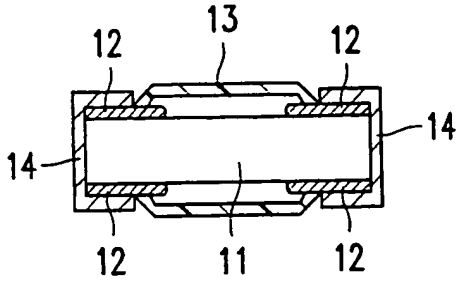

FIG. 3B

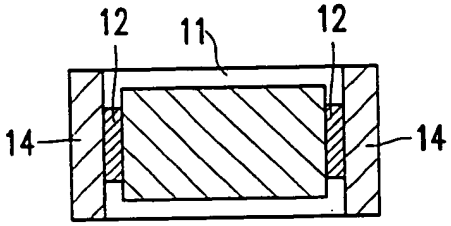

FIG. 3C

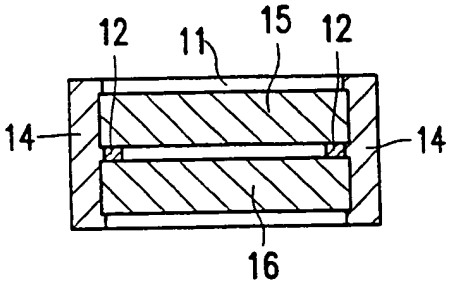

FIG. 3D

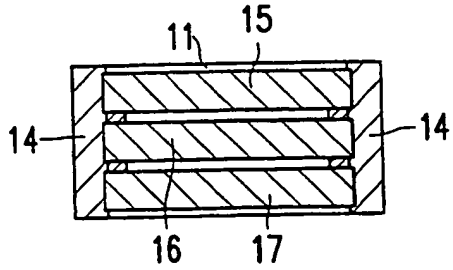

FIG. 3E

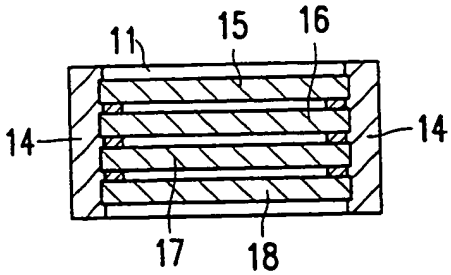

FIG. 3F

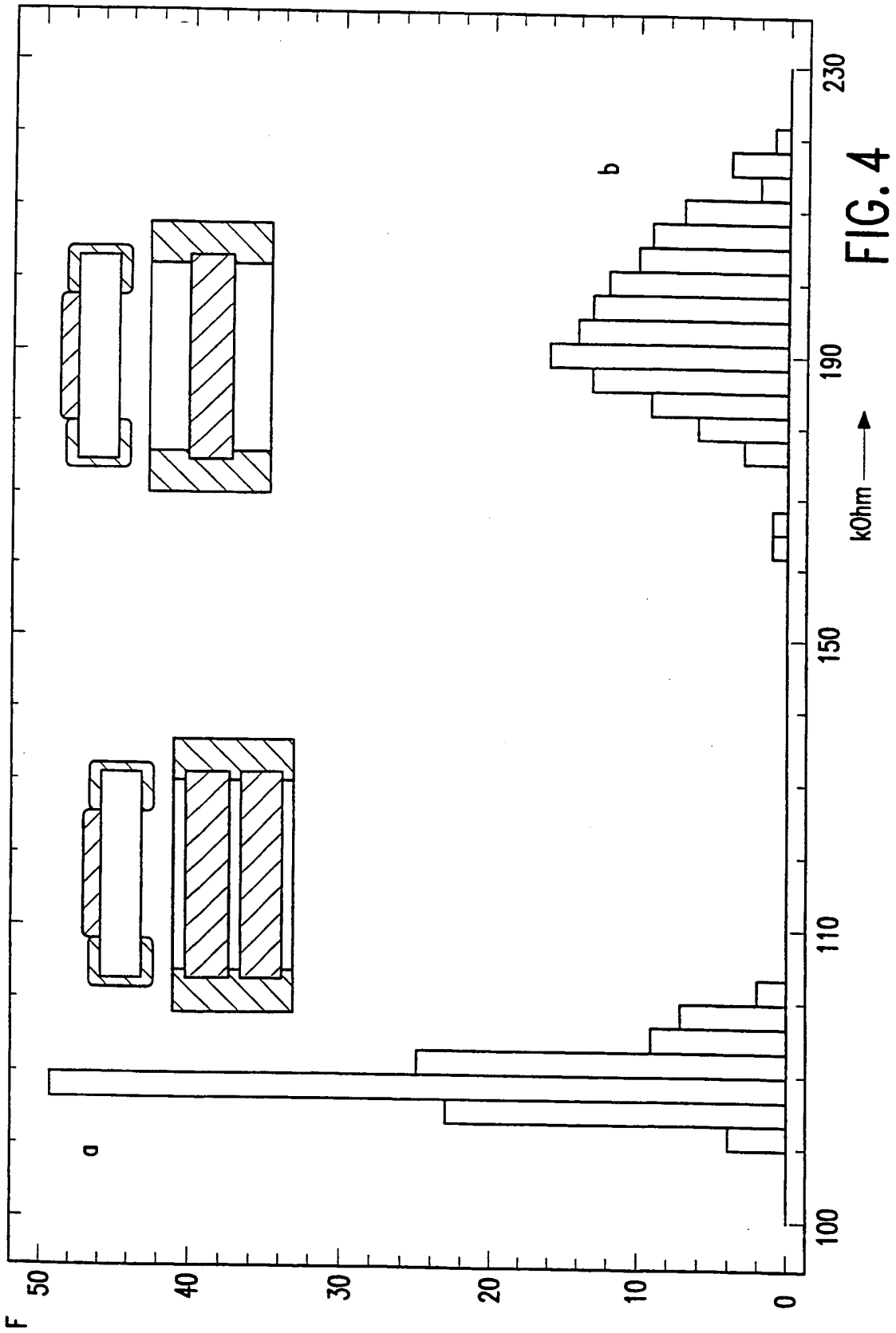

FIG. 4

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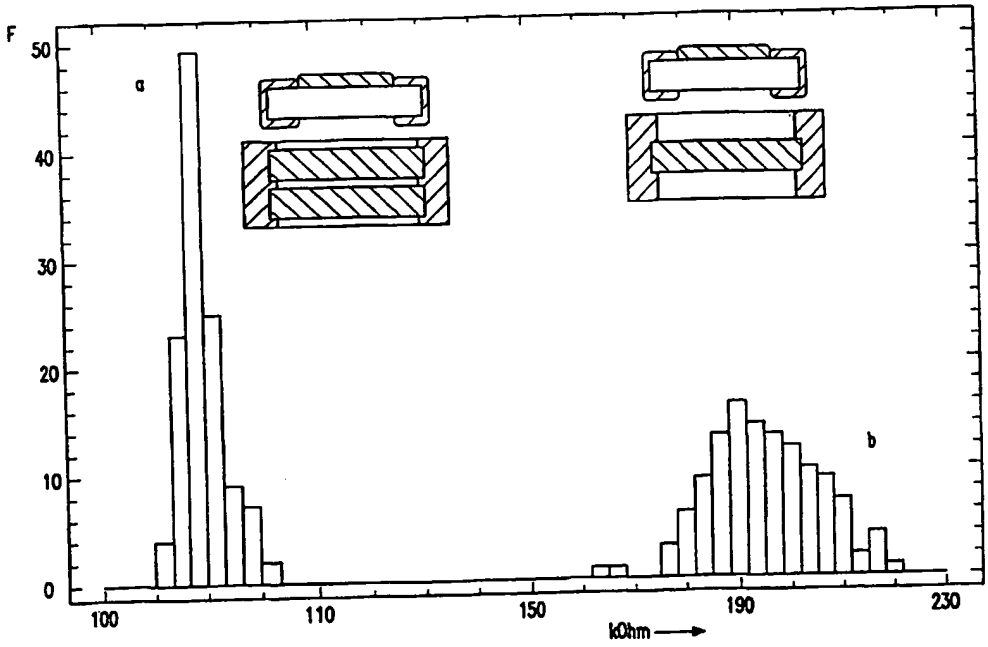

(57) Abstract

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

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According to International Patent Classification (IPC) or to both national classification and IPC

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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EPAT, WPI, JAPIO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0657898 A1 (PHILIPS ELECTRONICS N.V.), 14 June 1995 (14.06.95), figure 1, abstract --	1-6
X	JP 8172004 A (TAIYO YUDEN CO LTD), 2 July 1996 (02.07.96), abstract --	1-6
A	US 5258738 A (BRALT R. SCHAT), 2 November 1993 (02.11.93) --	1-6
A	JP 7153601 A (HOKURIKU TORYO KK), 16 June 1995 (16.06.95), abstract --	1-6

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search	Date of mailing of the international search report
3 Sept 1998	10 -09- 1998
Name and mailing address of the ISA/ Swedish Patent Office	Authorized officer

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 98/00133

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 7074002 A (KOA CORP.), 17 March 1995 (17.03.95), abstract ---	1-6
A	JP 9190902 A (ROHM CO LTD), 22 July 1997 (22.07.97), abstract ---	1-6
A	US 4803457 A (ROY W. CHAPEL, JR. ET AL), 7 February 1989 (07.02.89) --- ---	1-6

INTERNATIONAL SEARCH REPORT

Information on patent family members

27/07/98

International application No.
PCT/IB 98/00133

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0657898 A1	14/06/95	BE 1007868 A	07/11/95
		DE 69409614 D	00/00/00
		JP 7201529 A	04/08/95
JP 8172004 A	02/07/96	NONE	
US 5258738 A	02/11/93	DE 69213296 D,T	20/03/97
		EP 0509582 A,B	21/10/92
		JP 5121202 A	18/05/93
JP 7153601 A	16/06/95	NONE	
JP 7074002 A	17/03/95	NONE	
JP 9190902 A	22/07/97	NONE	
US 4803457 A	07/02/89	DE 3806156 A	08/09/88
		FR 2611402 A	02/09/88
		GB 2201553 A,B	01/09/88
		JP 63249301 A	17/10/88
		US 4907341 A	13/03/90

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(81) Designated State *(national)*: JP.

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10 December 1998

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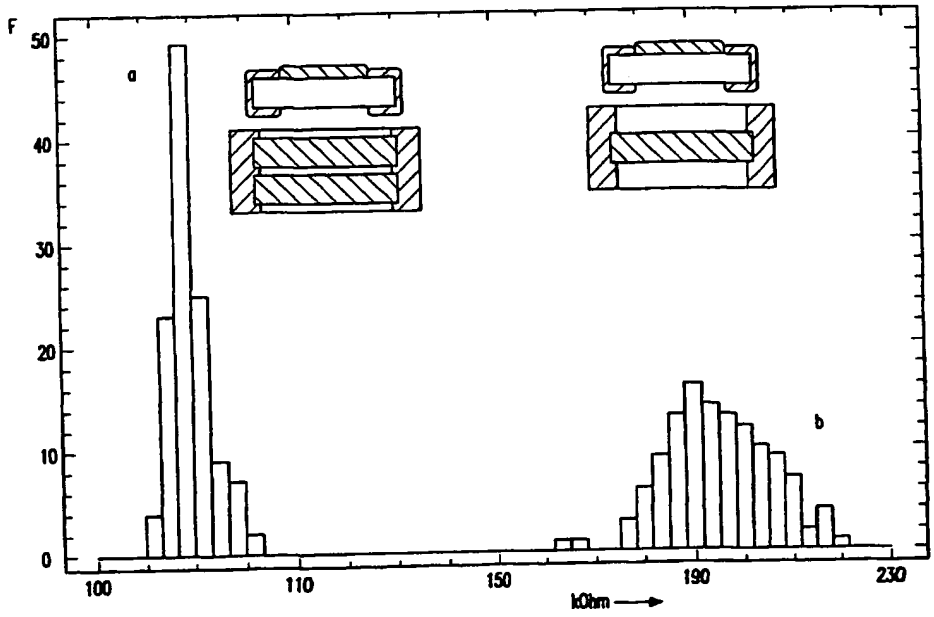
(54) Title: THICK FILM CHIP RESISTOR AND ITS MANUFACTURE



(57) Abstract: An improved method of manufacturing thick film chip resistors in mass production is described. By applying two or more resistance layers per chip resistor, less variance in the eventual resistance value is obtained if the resistors are manufactured in mass production using substrate plates. Less variance in the resistance value implies less trimming activity, which leads to a

WO 98/38652 A3

(15) **Information about Correction:**
see PCT Gazette No. 27/2001 of 5 July 2001, Section II

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Thick film chip resistor and its manufacture.

The invention relates to a method of manufacturing thick film chip resistors, said method comprising the following steps:

a. providing a number of contact layers on an electrically insulating substrate plate,

b. applying a number of thick film resistance layers on the substrate plate, each of said thick film resistance layers being in contact with two neighbouring contact layers,

c. fracturing the substrate plate into substrate rods,

d. applying end contacts to the contact layers, and

e. fracturing the rods into individual thick film resistors.

The invention also relates to a thick film chip resistor comprising an electrically insulating substrate a main surface of which is provided with two contact layers between which a thick film resistance layer is provided, each of said contact layers being provided with an end contact.

Both a method of manufacturing thick film chip resistors of the type mentioned in the opening paragraph and thick film chip resistors thus manufactured are known as such, f.i. from the American Patent Specification US 5.258.738 in the name of Applicant. This prior art document describes the use of alumina substrates of a specific type, which provides the fractured substrate rods so-called 'intergranular' fracture surfaces. The presence of such surfaces results in a better bonding between the substrate and the end contacts.

The known method of manufacturing thick film chip resistors suffers from an important disadvantage. It appears that the resistance values of the individual chip resistors which are obtained from a substrate plate are not (almost) identical, but show a certain variance around a mean resistance value. In order to obtain resistors with (almost) identical resistance values, a so-called trimming step is necessary. By trimming a small amount of the resistance material is removed, preferably by means of a laser, from the

resistance layer. Measuring the resistance value of the individual resistors and trimming them to a desired (higher) value results in resistors having (almost) identical resistance values. However, such trimming step is rather time-consuming and costly, and the trimming activity should therefor be as small as possible.

The main purpose of the invention is to reduce the mentioned disadvantage. The invention specifically aims at providing a method as mentioned in the opening paragraph, wherein the resistance values of individual thick film chip resistors obtained from one substrate plate show less variance around a desired resistance value.

These and other objects of the present invention are achieved by means of the method mentioned in the opening paragraph, which method in accordance with the invention is characterized in that the thick film resistance layer of each individual thick film chip resistor comprises at least two separate sub layers.

Experimental results have shown that separating the single thick film resistance layer as described in the prior art document into two or more sub layers results in a lower variance of the resistance values of the resistors around a certain mean value. This favourable effect causes a considerable reduction of the required trimming time and therefore results in a significant cost reduction of the known mass production process.

A favourable embodiment of the inventive method is characterized in that contact layers and thick film resistance layers are provided on both main surfaces of the substrate plate. This measure causes an advantageous increase of the power dissipation of thick film chip resistors having the same dimensions and electrical specifications. Chip resistors of the preferred construction can therefor better withstand high power applications.

Another favourable embodiment of the inventive method is characterized in that at least one of the sub layers comprises a resistive material having a positive TCR and in that at least one of the sub layers comprises a resistive material having a negative TCR. Thick film chip resistors of today generally suffer from the disadvantage that the absolute value of the TCR (temperature coefficient of the resistance) is rather high, typically 100 ppm/°C or more. For so-called low-ohmic resistors having a resistance value of 50 mΩ or less which are manufactured by thick film technology, the high TCR value of 500 ppm/°C or more causes an even more serious problem. By applying the proposed measure, TCR compensation is possible by using for a first sub layer a resistive material having a positive TCR and for a second sub layer a resistive material having a negative TCR. The TCR value

of the chip resistor will be between the TCR value of the individual sub layers.

The invention also relates to a thick film chip resistor comprising an insulating substrate a main surface of which is provided with two contact layers between which a thick film resistance layer is provided, each of said contact layers being contacted with an end contact. The inventive resistor is characterized in that the thick film resistance layer comprises at least two separate sub layers, which are at a distance of at least 0.05 mm. Using a smaller distance can result in undesired electrical contacts between the sub layers.

Preferably both main surfaces of the substrate are provided with a thick film resistance layer consisting of at least two separate sub layers, which are at a distance of at least 0.05 mm. Another favourable embodiment of the inventive resistor is characterized in that at least one of the sub layers comprises a resistive material having a positive TCR and in that at least one of the sub layers comprises a resistive material having a negative TCR.

The invention will be described in more detail by means of embodiments and the accompanying drawing, wherein

Figures 1 schematically shows different stages in the method according to the present invention

Figure 2 shows in a perspective view a detail of the substrate plate depicted in Figure 1

Figure 3 schematically shows a number of thick film chip resistors according to the present invention

Figure 4 shows in a histogram the results of the variance in resistance value which is measured in mass produced thick film chip resistors which are either manufactured in accordance with the present invention (a) or manufactured not in accordance with the present invention (b).

It is noted that the Figures are not drawn to scale.

The inventive method is described in more detail by means of Figs 1 and 2. Fig 1-A shows a top view of a substrate plate (1) of sintered Al_2O_3 having dimensions of about 108 x 78 x 0.54 mm^3. As shown in Fig 2, the substrate plate has been provided on the bottom surface with a first number of parallel, V-shaped fracture grooves (2) (rod grooves) and with a second number of parallel, V-shaped fracture grooves (3) (chip grooves). The

fracture grooves (2) and (3) extend substantially perpendicularly to each other and have a depth of approximately 0.1 mm. For clarity, only a few fracture grooves (2) and (3) are indicated with a dotted line in Fig 1.

On one of the main surfaces of substrate plate (1) as shown in Fig 1-A, longitudinal contact layers (4) (see Fig 2) are provided. These layers (4) can be provided by means of vacuum deposition techniques, such as f.i. sputtering and metal evaporation, but they are preferably provided by means of screen printing. Said screen printed contact layers, which contain for example Ag or Pd/Ag, are fired at 850° C for 1 hour. For clarity, only three contact layers are shown in Fig 2. It is noted, that the contact layers can also be constructed as small, discrete area's as shown in US 5.258.738.

Subsequently, thick film resistance layers are provided by means of screen printing, which layers are also fired at 850° C for 1 hour. The screen printing paste used for this purpose contains a mixture of conductive material (metal oxides as f.i. RuO_2 and/or $Pb_2Ru_2O_{6.5}$), glass fritt and minor additives such as binders. The resistance value of the resistance layer strongly depend of the exact composition of said paste.

According to an essential aspect of the present invention, these resistance layers comprise at least two separate sub layers (5,8) per individual chip resistor unit. For clarity, only two thick film resistance layers, each comprising two sub layers (5) and (8) per individual chip resistor unit are shown in Fig 2. It is noted that in principle the row order of steps a (providing contact layers) and step b (applying thick film resistance layers) can be reversed. However, the method in which the contact layers are provided on the substrate before the thick film resistance layer are applied is preferred.

In case that both sub layers contain the same resistance material, these layers can be printed in one and the same screen print step. However, according to a preferred embodiment of the present invention, the two sub layers are provided in two different print screen steps, using two types of resistance material. In the preferred embodiment, the one material comprises a resistive material having a positive TCR and the other material comprises a resistive material having a negative TCR. By using this embodiment of the invention, the TCR of the thick film chip resistor is relatively low, which is seen as an important advantage.

According to another preferred embodiment of the present invention, the same procedure of applying contact layers and resistance layers comprising at least two sub layers is also executed on the other main surface of the substrate plate.

After the contact layers and the thick film resistance layers have been

provided on one or both of the main surfaces of the substrate plate (1), a protective coating covering the resistance layers can be applied, f.i. by screen printing (not shown). Subsequently the substrate plate (1) is broken at the fracture grooves (2) (rod grooves) to form rods (6) (see Fig. 1-B). Next, a thin layer of Ni is deposited on the fracture surfaces by means of a vacuum deposition technique, such as f.i. evaporation or sputtering. Subsequently, a thicker layer of Ni is provided on said first layer by means of electroplating and a solder layer is applied onto the Ni-layers. It is also possible to use a dipping process for this purpose by dipping the fracture surfaces into a conductive paste which contains f.i. Ag or Ag/Pd, so that the fracture surfaces become covered by such paste. In such dipping process the substrate rods need to be fired for one hour at about 580°C in order to consolidate the conductive paste as a layer on the fracture surfaces. The thus formed end contacts are electrically conductively connected to the contact layers (4). Finally, the rods (6) are broken along the fracture grooves (3) (chip grooves) into individual thick film chip resistors. In Fig. 1-C, only a few of these resistors are schematically shown. In total, approximately 1800 thick film chip resistors having dimensions of 1.6 x 3.2 x 0.54 mm^3 can be manufactured from said Al_2O_3 substrate.

Fig 3 shows a cross sectional view and a top view of several types of thick film chip resistors, most of them according to the present invention. These resistors comprise an electrically insulating substrate (11) of alumina. Contact layers (12) and thick film resistance layers comprising at least two separate sub layers (vide infra) are present on one or both main surfaces of substrate (11) as depicted in Fig 3-A resp. Fig 3-B. A screen printed protective layer (13) fully cover the resistance layer. U-shaped metallic end contacts (14) are in electrical contact with contact layers (12).

Figs 3-C, 3-D, 3-E and 3-F give a top view of the resistor type as shown in Figs 3-A and 3-B. For clarity, the protective layer (13) is omitted in Figs 3-C, 3-D, 3-E and 3-F. As shown in these Figs, the resistance layer of various embodiments according to the present invention comprise respectively two, three or even four sub layers (15,16,17,18) having a thickness of about 10 micrometer. These layers are at a distance of at least 0.05 mm in order to avoid undesired electrical contact between neighbouring sub layers. The embodiment according to Fig 3-C having only a single resistance layer is not according to the present invention.

Figure 4 shows a histogram in which the frequency (F) of the individual resistors having a certain resistance value (kΩ) is depicted. For this experiment 120 resistors of the type shown in Fig 3-A were manufactured, either according to the presently claimed

inventive method (series a, left histogram) or not according to the present invention (series b, right histogram). The standard deviation of the a-series was about 4.4%. The standard deviation of the b-series was about 5.2%. These results (an 20% improvement) unambiguously demonstrate the effect of the present invention.

In summary, the present invention provides an improved method of manufacturing thick film chip resistors in mass production. By applying two or more resistance layers per chip resistor, less variance in the eventual resistance value is obtained if the resistors are manufactured in mass production using substrate plates. Less variance in the resistance value implies less trimming activity, which leads to a considerable cost reduction. Moreover, the use of two or more sub layers enables application of TCR compensation.

CLAIMS:

1. Method of manufacturing thick film chip resistors, said method comprising the following steps:

a. providing a number of contact layers on an electrically insulating substrate plate,

b. applying a number of thick film resistance layers on the substrate plate, each of said thick film resistance layers being in contact with two neighbouring contact layers,

c. fracturing the substrate plate into substrate rods,

d. applying end contact to the contact layers, and

e. fracturing the rods into individual thick film chip resistors,

characterized in that the thick film resistance layer of each individual thick film chip resistor comprises at least two separate sub layers.

2. Method according to claim 1, characterized in that contact layers and thick film resistance layers are provided on both main surfaces of the substrate plate.

3. Method according to claim 1 or 2, characterized in that at least one of the sub layers of the thick film resistance layer comprises a resistive material having a positive TCR and in that at least one of the sub layers comprises a resistive material having a negative TCR.

4. Thick film chip resistor comprising an electrically insulating substrate a main surface of which is provided with two contact layers between which a thick film resistance layer is provided, each of said contact layers being provided with an end contact, characterized in that the thick film resistance layer comprises at least two separate sub layers, which are at a distance of at least 0.05 mm.

5. Thick film chip resistor as defined in claim 4, characterized in that both main surfaces of the substrate are provided with a thick film resistance layer comprising at least two separate sub layers, which are at a distance of at least 0.05 mm.

6. Thick film chip resistor as defined in claim 4 or 5, characterized in that at least one of the sub layers comprises a resistive material having a positive TCR and in that at least one of the sub layers comprises a resistive material having a negative TCR.

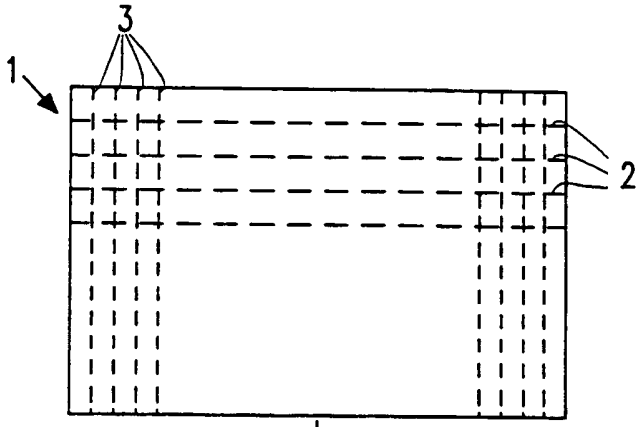


FIG. 1A

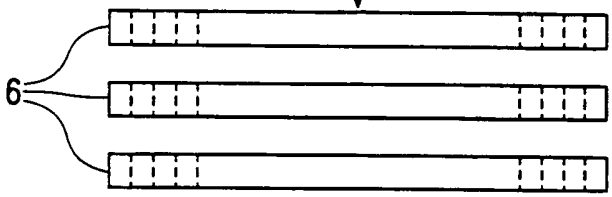


FIG. 1B

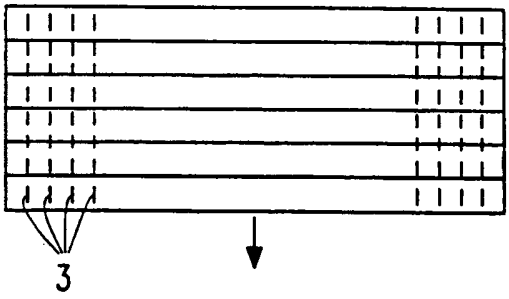


FIG. 1C

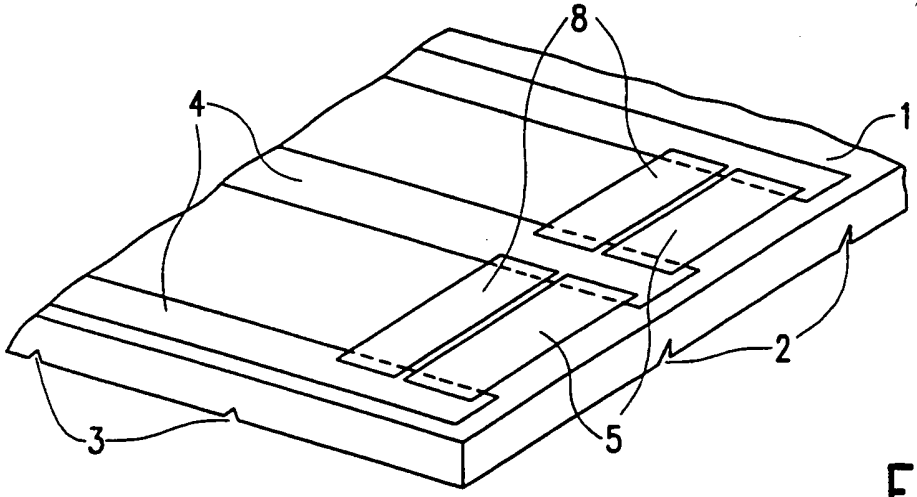


FIG. 2

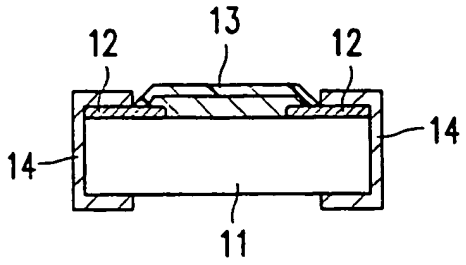


FIG. 3A

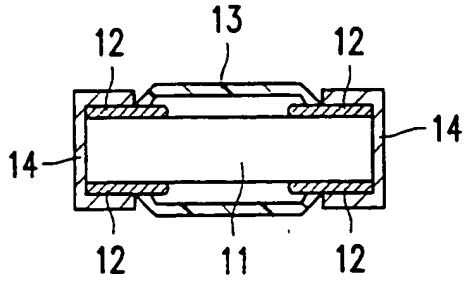


FIG. 3B

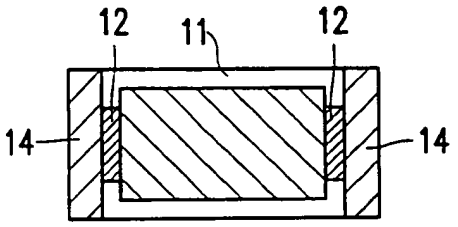


FIG. 3C

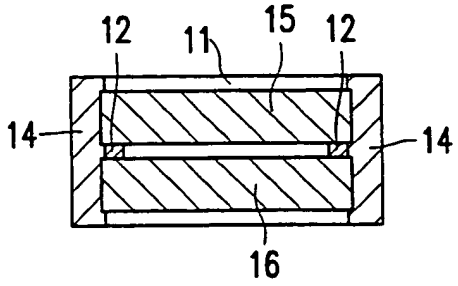


FIG. 3D

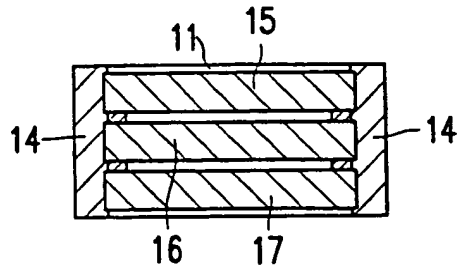


FIG. 3E

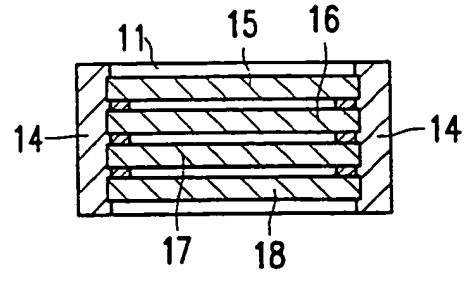


FIG. 3F

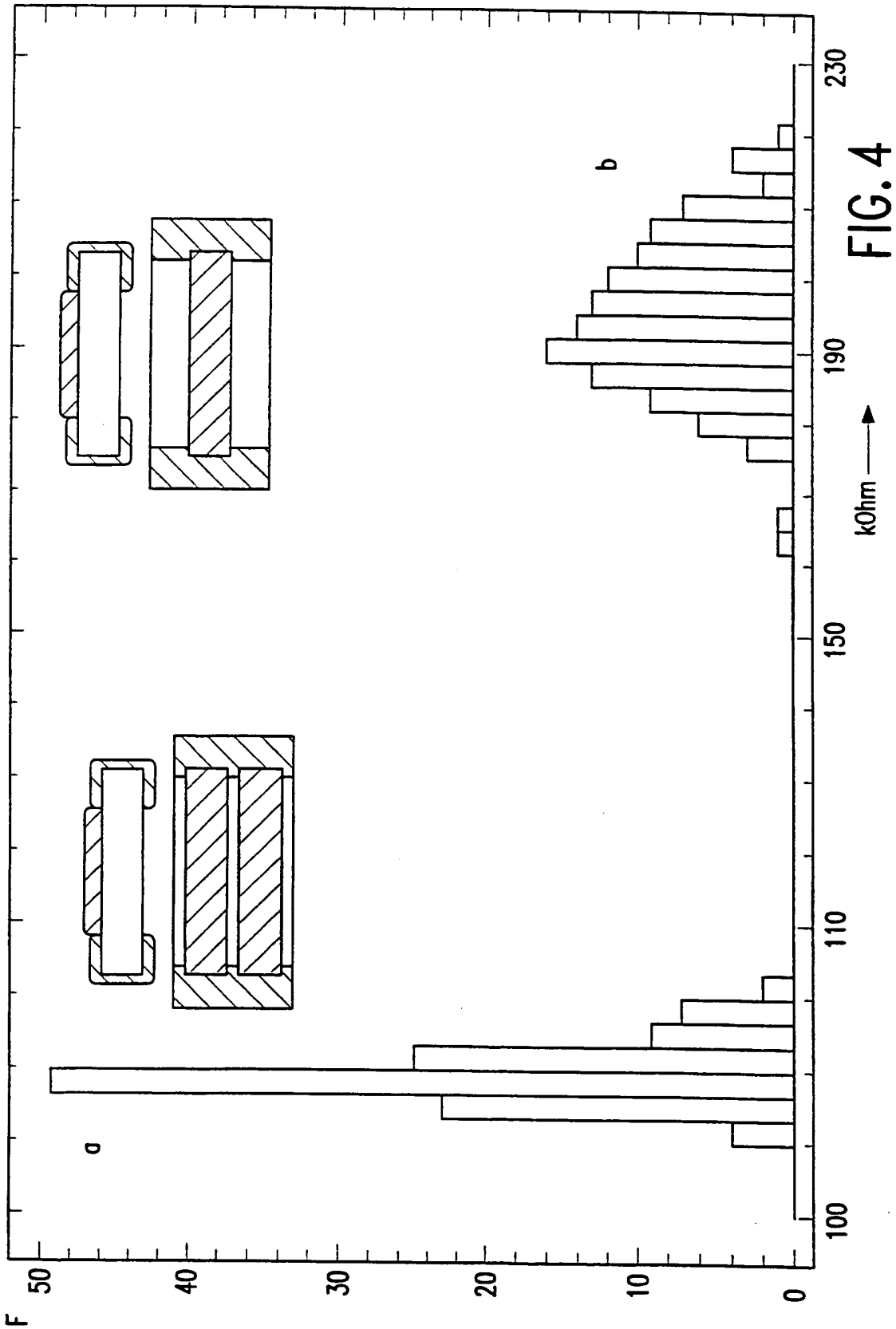


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 98/00133

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01C 17/065
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPAT, WPI, JAPIO

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 Sept 1998	10 -09- 1998
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM	Authorized officer Benny Andersson

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 98/00133

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		EP 0509582 A,B	21/10/92
		JP 5121202 A	18/05/93
JP 7153601 A	16/06/95	NONE	
JP 7074002 A	17/03/95	NONE	
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		US 4907341 A	13/03/90